CLAIMS

1. A thin film transistor comprising:

an insulating substrate;

a polycrystalline silicon island formed on said insulating layer, a grain size of said polycrystalline silicon island being elongated along one direction; and

a source region, a channel region and a drain region arranged in said polycrystalline silicon island in parallel with said direction.

2. The thin film transistor as set forth in claim 1, wherein said insulating substrate comprises a glass substrate.

3. A method for manufacturing a thin film transistor, comprising the steps of:

forming an amorphous silicon layer on an insulating substrate;

irradiating said amorphous silicon layer with a laser line beam along a first direction, so that a portion of said amorphous silicon layer irradiated with said laser line beam is converted into a polycrystalline silicon layer;

patterning said polycrystalline silicon layer into a polycrystalline silicon island; and

forming a source region, a channel region and a drain region of said thin film transistor in said polycrystalline silicon island.

4. The method as set forth in claim 3, wherein said source region, said channel region and said drain region of said thin film transistor are arranged along a second direction perpendicular to said first direction.

5. The method as set forth in claim 3, wherein

said laser line beam irradiating step irradiates said amorphous silicon layer with said laser line beam, so that polycrystalline silicon is grown from portions of said amorphous silicon layer close to edges of said laser line beam to a portion of said amorphous silicon layer close to a center of said laser line beam.

said polycrystalline silicon layer being divided into two regions at a line corresponding to the center of said laser line beam.

6. The method as set forth in claim 5, wherein said polycrystalline silicon island is located within either of the two regions of said polycrystalline silicon layer.

7. The method as set forth in claim 3, wherein said insulating substrate comprises a glass substrate.

8. A method for manufacturing a thin film transistor, comprising the steps of:

forming an amorphous silicon layer on an insulating substrate;

irradiating said amorphous silicon layer with a laser line beam along a first direction, so that polycrystalline silicon is grown from portions of said amorphous silicon layer close to edges of said laser line beam to a portion of said amorphous silicon layer close to a center of said laser line beam, thus forming a polycrystalline silicon layer divided into two regions at a line corresponding to the center of said laser line beam;

patterning said polycrystalline silicon layer into a polycrystalline silicon island; and

forming a source region, a channel region and a drain region of thin film transistor in

either of the two regions of said polycrystalline silicon island along a second direction perpendicular to said first direction.

9. The method as set forth in claim 8, wherein said insulating substrate comprises a glass substrate.

10. A method for manufacturing a P-channel type thin film transistor and an N-channel type, comprising the steps of:

forming an amorphous silicon layer on an insulating substrate;

irradiating said amorphous silicon layer with a plurality of laser line beams along first direction, so that portions of said amorphous silicon layer irradiated with said laser line beams are converted into a plurality of polycrystalline silicon layers;

patterning each of said polycrystalline silicon layers into a plurality of polycrystalline silicon islands; and

forming a source region, a channel region and a drain region of said P-channel type thin film transistor in one of said polycrystalline silicon islands of one of said polycrystalline silicon layers and a source region, a channel region and a drain region of said N-channel thin film transistor in one of said polycrystalline silicon islands of the other of said polycrystalline silicon layers.

11. The method as set forth in claim 10, wherein said source region, said channel region and said drain region of said P-channel type thin film transistor said source region, said channel region and said drain region of said N-channel thin film transistor are arranged along a second direction perpendicular to

said first direction.

12. The method as set forth in claim 10, wherein said laser line beam irradiating step irradiates said amorphous silicon layer with said laser line beams, so that polycrystalline silicon is grown from portions of said amorphous silicon layer close to edges of each of said laser line beams to portions of said amorphous silicon layers close to centers of each of said laser line beams.

each of said polycrystalline silicon layers being divided into two regions at a line corresponding to the centers of said laser line beams.

13. The method as set forth in claim 12, wherein each of said polycrystalline silicon islands is located within either of the two regions of one of said polycrystalline silicon layers.

14. The method as set forth in claim 10, wherein said insulating substrate comprises a glass substrate.

15. A method for manufacturing a P-channel thin film transistor and an N-channel thin film transistor, comprising the steps of:

forming an amorphous silicon layer on an insulating substrate;

irradiating said amorphous silicon layer with a plurality of laser line beams along a first direction, so that polycrystalline silicon is grown from portions of said amorphous silicon layer close to edges of each of said laser line beams to portions of said amorphous silicon layer close to a center of each of said laser line beams, thus forming a plurality of polycrystalline silicon layers each divided into two regions at a line corresponding to the center of each of said laser line beams;

patterning either of the two regions of

each of said polycrystalline silicon layers into a plurality of polycrystalline silicon islands and

forming a source region, a channel region and a drain region of said P-channel type thin film transistor in either of the two regions of one of said polycrystalline silicon islands belonging to one of said polycrystalline silicon layers and a source region, a channel region and a drain region of said N-channel thin film transistor in either of the two regions of one of said polycrystalline silicon islands belonging to the other of said polycrystalline silicon layers along a second direction perpendicular to said first direction.

16. The method as set forth in claim 15, wherein said insulating substrate comprises a glass substrate.

17. An image input apparatus comprising:

an insulating substrate;

a plurality of polycrystalline silicon islands formed on said insulating substrate;

a plurality of pixels each including thin film transistors and a photodiode formed above said thin film transistors,

each of said thin film transistors having a source region, a channel region and a drain region formed in one of said polycrystalline silicon islands.

18. The apparatus as set forth in claim 17, wherein a grain size of said polycrystalline silicon islands is elongated along one direction,

said source region, said channel region and said drain region of each of said film transistors being in parallel with said direction.

19. The apparatus as set forth in claim 17, wherein said insulating substrate comprises a glass

substrate.

20. The apparatus as set forth in claim 17, further comprising:

an additional photodiode, formed on said insulating substrate and surrounding all of said pixels, for detecting whether or not light is incident to all of said pixels; and

a reset circuit, connected between said additional photodiode and all of said pixels, for generating a reset signal when said additional photodiode detects that light is incident to all of said pixels,

so that said photodiode of each of said pixels is reset by said reset signal.

21. The apparatus as set forth in claim 17, wherein said photodiode comprises a Schottky barrier diode.

22. The apparatus as set forth in claim 17, wherein said photodiode comprises a PIN diode.

23. The apparatus as set forth in claim 20, wherein said additional photodiode comprises a Schottky barrier diode.

24. The apparatus as set forth in claim 20, wherein said additional photodiode comprises a PIN diode.